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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,213	02/27/2004	Chiung-Pin Wang	BHT-3167-179	4703

7590 11/09/2005

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EXAMINER	
CHEN, WEN YING PATTY	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/787,213	WANG, CHIUNG-PIN
	Examiner	Art Unit
	Wen-Ying P. Chen	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's Amendment filed on Oct. 7, 2005 has been received and entered. Claim 9 is cancelled per the Amendment filed. Therefore, claims 1-8, 10-16 are now pending in the current application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. (US 2004/0051836A1) in view of Nakashima (US 6049365).

With respect to claim 1: Jung et al. disclose in Figure 5 a flat panel display comprising: a glass substrate (element 110), which is divided into a displaying area (element D) and a

surrounding frame area (element S_2), wherein the displaying area further comprising a plurality of pixel devices, each pixel device comprising a thin film transistor (TFT) (element 120) utilized as a switch;

a plurality of first conductive lines (element CL_1), substantially parallel to each other, formed atop the frame area for controlling a portion of the TFTs;

a dielectric layer (element 127) covering the first conductive lines; and a plurality of second conductive lines (element CL_2), substantially parallel to each other, formed on top of the dielectric layer for controlling the other TFTs.

Jung et al. further disclose in Figure 5 that the second conductive lines (element CL_2) are connected to the gate lines (element GL) through a contact hole (element 127a) and a passivation layer (element 130) formed atop the frame area for covering the second conductive lines, but fail to disclose that a connecting structure, formed on the frame area, having a first plug penetrating the dielectric layer and the passivation layer and further connecting to a gate line, a second plug penetrating the passivation layer and further connecting to the second conductive line, and an interconnecting line formed atop the passivation layer connecting to the first plug and the second plug.

However, Nakashima discloses in Figure 1(b) and Column 5 lines 32-52 that a passivation layer (102) is formed atop the frame area for covering second conductive lines (element 61) and a connecting structure (element 17), formed on the frame area, having a first plug (element 103d) penetrating the dielectric layer (element 23) and the passivation layer (element 102) and further connecting to a gate line (element 60), a second plug (element 103c) penetrating the passivation layer and further connecting to the second conductive line (element

61), and an interconnecting line (element 54) formed atop the passivation layer connecting to the first plug and the second plug.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a flat panel display as taught by Jung et al. wherein the second conductive line and the gate line is connected by a connecting structure as taught by Nakashima, since Nakashima teaches that the interconnecting line is tend to be formed of a more corrosion resistance and low resistivity material than that of the wiring lines, thus helps prevent wire shortage between the conductive line and the gate line (Column 2, lines 3-15).

As to claims 2 and 4: Jung et al. further disclose that the first conductive lines, the gate lines and the gate electrodes of the TFTs are formed in a metal layer and the first conductive lines are formed such that they are positioned along a boundary of the displaying area with a predetermined interval (Paragraphs 0065 and 0066).

As to claims 3 and 5: Jung et al. further disclose that the second conductive lines and the source/drain electrodes of the TFTs are formed in a metal layer and the second conductive lines are formed such that they are positioned along a boundary of the displaying area with a predetermined interval (Paragraphs 0074, 0075 and 0078).

As to claim 6: Jung et al. further disclose that the dielectric layer is formed of silicon nitride (Paragraph 0067).

As to claims 7 and 8: Jung et al. disclose in Figures 6A-6F the method of forming a flat panel comprising the steps of:

forming a plurality of gate lines (element GL) and a plurality of first conductive lines (element CL_1) on a glass substrate (element 110) by first forming a metal layer (element 111)

and then by etching of the metal layer, wherein the first conductive lines are connected to the gate lines;

forming a dielectric layer (elements 122 and 127) to cover the gate lines and the first conductive lines;

forming a second metal layer (element 114) over the dielectric layer (elements 122 and 127);

etching the second metal layer to form the sources (element 125), drains (element 126), and second conductive lines (element CL_2); and

forming a passivation layer (element 130) to cover the sources, the drains, and the second conductive lines.

Jung et al. disclose that the second conductive lines (element CL_2) are connected to the gate lines (element GL) through a contact hole (element 127a) formed in the dielectric layer, but fail to disclose a plurality of openings exposing the second conductive lines and the rest of the gate lines are formed by etching the passivation layer, and forming a plurality of connecting structures on the passivation layer for filling the openings to connect the second conductive lines and rest of the gate lines.

However, Nakashima discloses in Figure 1(b) and Column 5 lines 32-52 that a passivation layer (102) is formed covering second conductive lines (element 61) and a connecting structure (element 17), having openings (elements 103c and 103d) exposing the second conductive lines and the gate lines, and forming an interconnecting line (element 54) for filling the openings to connect the second conductive lines and rest of the gate lines.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a flat panel display as taught by Jung et al. wherein the second conductive line and the gate line is connected by a connecting structure as taught by Nakashima, since Nakashima teaches that the interconnecting line is tend to be formed of a more corrosion resistance and low resistivity material than that of the wiring lines, thus helps prevent wire shortage between the conductive line and the gate line (Column 2, lines 3-15).

As to claims 10-12: Jung et al. further disclose in Figure 6F that the method comprises steps of forming the gate lines (element GL) in a displaying area (element D) and the first and second conductive lines (elements CL_1 and CL_2) in a surrounding frame area (element S_2), wherein the first and second conductive lines are positioned with a predetermined interval.

As to claim 13: Jung et al. further disclose in Paragraph 0067 that the dielectric layer is formed of silicon nitride.

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. (US 2004/0051836A1) in view of Nakashima (US 6049365) further in view of Hinata (US 2001/0022644).

Jung et al. disclose in Figure 1 a liquid crystal display comprising a color filter layer (element 200), a liquid crystal layer (element 300), a TFT panel (element 100), and in Figure 2 a driving circuit (element 150) having connection with the gates of the TFTs through conductive lines. Jung et al. further disclose in Figures 5, and 6A-6G that the TFT panel further comprising: a rectangular glass substrate (element 110) divided into a displaying area (element D) and a surrounding frame area (element S_2), a plurality of pixel devices each device comprising a thin

film transistor (TFT) (element 120) utilized as a switch; a plurality of first conductive lines (element CL_1) formed in the frame area positioned with a predetermined interval, wherein the first conductive lines and the gate electrodes are formed in a metal layer (element 111); a dielectric layer (element127) formed of silicon nitride (Paragraph 0067) deposited on top of the first conductive lines at the frame area; and a plurality of second conductive lines (element CL_2) formed on top of the dielectric layer and positioned with a predetermined interval having connection to the rest of the gate lines, wherein the second conductive lines and the source and drain electrodes are formed in a metal layer (element 114).

Jung et al. further disclose in Figure 5 that the second conductive lines (element CL_2) are connected to the gate lines (element GL) through a contact hole (element 127a) and a passivation layer (element 130) formed atop the frame area for covering the second conductive lines, but fail to disclose that a connecting structure, formed on the frame area, having a first plug penetrating the dielectric layer and the passivation layer and further connecting to a gate line, a second plug penetrating the passivation layer and further connecting to the second conductive line, and an interconnecting line formed atop the passivation layer connecting to the first plug and the second plug and that the flat panel comprises a backlight module.

However, Nakashima discloses in Figure 1(b) and Column 5 lines 32-52 that a passivation layer (102) is formed atop the frame area for covering second conductive lines (element 61) and a connecting structure (element 17), formed on the frame area, having a first plug (element 103d) penetrating the dielectric layer (element 23) and the passivation layer (element 102) and further connecting to a gate line (element 60), a second plug (element 103c) penetrating the passivation layer and further connecting to the second conductive line (element

61), and an interconnecting line (element 54) formed atop the passivation layer connecting to the first plug and the second plug and Hinata discloses in Figure 2 a liquid crystal display, which comprises of a back light module (element 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a flat panel display as taught by Jung et al. wherein the second conductive line and the gate line is connected by a connecting structure as taught by Nakashima, since Nakashima teaches that the interconnecting line is tend to be formed of a more corrosion resistance and low resistivity material than that of the wiring lines, thus helps prevent wire shortage between the conductive line and the gate line (Column 2, lines 3-15) and to include a backlight module as taught by Hinata so that illumination of the display can be provided with the light source.

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Ying P. Chen whose telephone number is (571)272-8444. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Ying P Chen
Examiner
Art Unit 2871

WPC
11/04/05

ROBERT KIM
SUPERVISORY PATENT EXAMINER